UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/716,977	11/20/2000	Alfred Earl Dunlop	13-6	1939

7590 11/19/2004

Kevin M. Mason
Rayan, Mason & Lewis, LLP
Suite 205
1300 Post Road
Fairfield, CT 06430

EXAMINER	
ZHENG, EVA Y	
ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/716,977	DUNLOP ET AL.	
	Examiner	Art Unit	
	Eva Yi Zheng	2634	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 10/4/04 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: *10,22,31,35 and 36*.

   Claim(s) rejected: *1-9,11-21,23-30 and 32-34*.

   Claim(s) withdrawn from consideration: _____.

8. ☒ The drawing correction filed on *17 May 2004* is a)☒ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

SHUWANG LIU
PRIMARY EXAMINER

Continuation of 5. does NOT place the application in condition for allowance because: The argument offered by the Applicant with regard to claims have been addressed sufficiently in the Examiner's Office action and the Examiner's position remains unchanged. (Please see attachment).

Attachment

Applicant's Amendment After Final Rejection arguments filed on October 4, 2004, have been fully considered but they are not persuasive. Examiner has thoroughly reviewed Applicant's arguments but firmly believes that the cited reference reasonably and properly meet the claimed limitation as rejected.

Applicant's argument – "Mittel et al. does not disclose or suggest that the bias signal generate by a first PLL is not used to bias a second PLL in a second mode."

Examiner's response - Mittel et al. disclose a first PLL (202 in Fig. 6) for generating an oscillator signal (212 in Fig. 6) and for generating a bias signal (214 in Fig. 6); a second PLL circuit (206 in Fig. 6) generating a clock output signal (216 in Fig. 6), wherein said second PLL circuit is controlled by said bias signal (214 in Fig. 6) generated by said first PLL circuit in a first mode and wherein said second PLL circuit has a second mode (147 in Fig. 6) wherein said second PLL has an initial frequency determined by said bias signal and whereby said second PLL substantially instantaneously adjusts said clock output signal to phase changes of data in an input data stream without utilizing said bias signal.

Mittel et al. clearly and explicitly disclose that the signal 214 is set to bias point only during power up (Col 6, L44-47). This means that signal 214 is used by the second PLL (206) only during power up condition. When the power is down, the first PLL (202) will not use bias signal (214). Instead, first PLL will control the second PLL (206) directly for generating a clock output signal. Therefore, the bias signal generate by a first PLL is not used to bias a second PLL in a second mode.